A Large-Signal Physical MESFET Model for Computer-Aided Design and Its Applications

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***Abstract*—A quasi-static, large-signal MESFET circuit model has been developed. It is based on a comprehensive quasi-two-dimensional semiclassical device physical simulation where its unique formulation and efficiency make it suitable for the computer-aided design of nonlinear MESFET subsystems. Using this approach the semiconductor equations are reduced to a consistent one-dimensional approximation requiring substantially less computing resources than a full two-dimensional simulation. CPU time is typically reduced by a factor of 1000. A single/two-tone harmonic balance analysis procedure which employs the describing frequency concept has also been developed and combined with the MESFET model. Numerical load-pull contours, as well as intermodulation distortion contours, have been simulated and comparison of these with measured results validates the approach taken.**

I. Introduction

GaAs MESFET's are the fundamental building block for both discrete and monolithic microwave integrated circuits (MMIC's). The requirements to minimize development costs and optimize device–circuit interaction have led to an increased interest in physical device models which intrinsically relate the basic material and geometrical parameters of a device to its dc and RF performance. Moreover, the trend toward higher frequency of operation (shorter gate length devices) requires models capable of describing non-equilibrium transport phenomena (hot-electron effects). Many two-dimensional physical simulations which provide insight into the device operation have been proposed [1]–[5], but these require large computing resources and are not, as yet, generally applicable in the design process. The model presented here is based on a description of the carrier dynamics (transport equations) derived from the Boltzmann equation [6].

The validity of the model for both dc and small-signal (S-parameter) conditions has been assessed previously [7], [8] and the object of this paper is the application of the model to the computer-aided design (CAD) of nonlinear microwave subsystems when device–circuit interaction can be addressed and sensitivity analysis performed as a function of the basic device parameters. To this end a quasi-static, large-signal MESFET model has been derived from the simulation and combined with an efficient single/two-tone harmonic balance analysis procedure in order to simulate load-pull and intermodulation distortion contours.

The basis of the quasi-two-dimensional physical simulation is described in Section II and the quasi-static, large-signal MESFET circuit model is presented in Section III together with simulated results for a power device used throughout the work. Section IV describes the single/two-tone nonlinear analysis procedure developed and this is followed by experimental results, in Section V.

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II. Quasi-Two-Dimensional Physical MESFET Simulation

A. Transport Equations

The physical simulation is based on the four semiclassical semiconductor equations coupled with analytical expressions for the MESFET channel. The model accounts for process-related parameters (geometry, recess depth, material parameters, doping profile, etc.), surface depletion effects, substrate conduction, contact resistivities, avalanche breakdown, and forward gate conduction [8]. A more complete carrier transport model than in previous quasi-two-dimensional simulations [9], [10] is employed and the Poisson and current continuity equations are solved together with the energy and momentum conservation equations. The solution of the latter allows hot-electron effects (velocity overshoot) to be simulated, thus making the model also suitable for short-gate-length MESFET's.

The basic simplifying assumptions for the MESFET channel, based on the results of full two-dimensional simulations, are

i) no current flows through the depleted region,
ii) current density is one-dimensional,
iii) potential contours in the undepleted part of the active channel and in the substrate are all parallel and are perpendicular to the active layer/substrate interface.

Fig. 1 shows the model geometry which derives from these. Approximation iii) provides continuity of potential,

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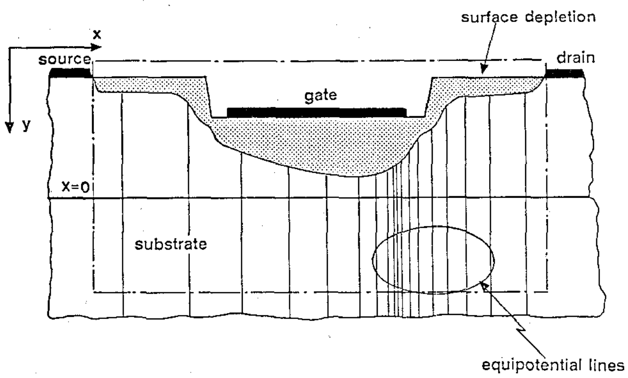


Fig. 1. Model geometry for the quasi-two-dimensional model.

with charge being continuous across the interface, leading to a substrate charge n_s and consequently a substrate current. This is represented in the model by an equivalent channel thickness to account for electrons being injected into the substrate [8].

For this quasi-two-dimensional model, the two-dimensional semiconductor equations are reduced to a one-dimensional set consistent with the approximations described, taking the forms given below.

Poisson's equation is

$$\frac{\partial E_x y}{\partial x} = \frac{q}{\epsilon_r}(N_D - n)y \tag{1}$$

where E_x is the longitudinal component of the electric field, y is the equivalent conductive channel height, N_D is the doping level, and n is the electron density. Equation (1) is obtained by applying Gauss' law to an incremental volume element. It assumes that the electric field flux across the gate depletion region is zero and that the electric field has no transversal component in the substrate.

The equation for current continuity is

$$\frac{\partial nyv}{\partial x} + \frac{\partial ny}{\partial t} = 0 \tag{2}$$

where v is the electron velocity (assumed one-dimensional). Following Cook and Frey's work [3], the equations for momentum and energy conservation are described by

$$v = \mu\left[E_x - \frac{2}{3}K\frac{\partial W}{\partial x} - \frac{2}{3}(W - G_U\Delta_{LU})\frac{1}{n}\frac{\partial n}{\partial x}\right] \tag{3}$$

$$\frac{\partial W}{\partial x} = \frac{1}{1+\frac{2}{3}K}\left[E_x - \frac{W - W_0}{v\tau_W}\right] \tag{4}$$

where μ is the electron mobility, τ_W the energy relaxation time (both functions of the average electron energy W), and W_0 is the lattice energy. G_U (the upper valley fraction) and $K(K = \partial G_U/\partial W)$ account for the two-valley nature of GaAs and Δ_{LU} is the lower to upper valley energy gap (0.36 eV for GaAs). Equation (3) shows the electron velocity in its drift and diffusion form. The last term in (3) can be neglected, however, since it has been shown that longitudinal thermal diffusion is dominant in the hot electron range [3]. The energy conservation equation (4) states that the electron energy flow balances the energy loss due to collisions together with the energy gain by Joule heating due to the electric field. In equations (3) and (4) energy-dependent material parameters are obtained by curve fitting the results of Monte Carlo simulations [9].

B. MESFET Simulation

Using the finite difference technique, the MESFET channel is divided into incremental sections of length Δx, and a backward difference scheme, which follows the carrier displacement from source to drain, is applied. The required boundary conditions are the gate voltage and the source current. The discretized form of (1) to (4) (no time dependence in (2)) is combined with analytical expressions for both the gate and the surface depletion depth resulting in a quadratic equation for the electron velocity at each mesh point in the MESFET channel. The coefficients in this equation are all functions of the average electron energy, so that an iterative procedure is necessary. Generally not more than five iterations are required to guarantee satisfactory convergence. The main consequence of this efficiency is that the typical CPU time for a full channel simulation is of the order of 0.6 s on a VAX 8600, representing a reduction by a factor of approximately 1000 compared to a full two-dimensional simulation. Typical simulated results for the device used in this work can be found elsewhere [8].

III. Quasi-Static Large-Signal MESFET Equivalent Circuit Model

The drive toward large-scale integration, often using monolithic techniques, requires efficient CAD tools capable of predicting and optimizing device and circuit large-signal performance prior to fabrication.

An approach whereby a quasi-static, large-signal MESFET equivalent circuit model is derived from a numerical simulation has been developed. From Poisson's and current continuity equations one can identify the basic phenomena that need to be accounted for when developing a MESFET circuit model. Substitution of (1) in (2) provides

$$\frac{\partial qnyv}{\partial x} - \epsilon_r\frac{\partial}{\partial t}\left[\frac{\partial E_x y}{\partial x}\right] + q\frac{\partial N_D y}{\partial t} = 0. \tag{5}$$

Equation (5) shows that at every point in the channel the current is formed by a conduction component and a displacement counterpart. The latter is caused by the capacitive nature of both the domain created in the device channel (second term in (5)) and the expansion of the gate depletion region (third term). Under the quasi-static assumption the conduction and displacement currents give rise to lumped nonlinear current sources and capacitors, respectively.

For each simulated point of the device characteristics (I_{DS} versus V_{DS}), small perturbations of the gate voltage and/or source current (the independent variables for the physical simulation) provide the MESFET's equivalent circuit element values G_m, G_{DS} (represented by I_{DS}), C_{GS}, C_{DG}, and C_{DOM}, shown in Fig. 2 The voltage and charge

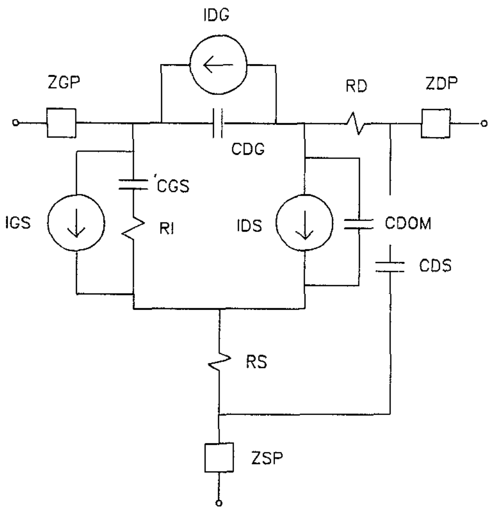


Fig. 2. MESFET equivalent circuit model.

distributions within the MESFET channel made available by the physical simulation enables these incremental parameters to be properly calculated. The source and drain resistances (R_S and R_D) as well as the drain–source capacitance (C_{DS}) are assumed to be bias independent, and the gate, source, and drain contact resistances (R_{GC}, R_{SC}, and R_{DC}) are calculated within the simulation from information (resistivities, metallization thicknesses, and pad areas) supplied for the Schottky and ohmic contacts. The gate charging resistance (R_I) is assumed to be inversely proportional to the gate–source capacitance and proportional to the electron transit time under the gate (τ), which is also calculated by the simulation. It is important to note that the gate–source capacitance C_{GS} is made up of two contributions arising from the gate depletion region and from the domain formed in the channel.

Fig. 3 shows the bias-dependent equivalent circuit element values for an NE9000 series 0.5 μm power GaAs MESFET. A full set of results can be generated in less than 3 minutes on a VAX 8600. Data on the device structure, which were supplied by NEC, have been used for full two-dimensional simulations and for comparing simulated load-pull results with those obtained by measurements [11].

IV. The Single/Two-Tone Harmonic Balance Analysis Procedure

In order to assess the validity of the large-signal MESFET equivalent circuit model, this has been combined with a harmonic balance analysis routine capable of handling single-frequency as well as two-tone excitations. Intermodulation distortion (IMD) contouring [12], as well as load-pull contouring, can then be simulated, providing a powerful link between the device technology/fabrication environment and the subsystem design state.

The harmonic balance technique is a well-established procedure and has been extensively addressed in the literature ([13], [14], and references therein). The procedure employed here is based on a relaxation method using a secant solver scheme [15]. Its main advantages rely on the fact that no Jacobians are needed and that for mildly nonlinear circuit operation (such as power amplifiers) the scheme is very efficient, requiring very few iterations and very small memory requirements.

With respect to the frequency-domain analysis of nonlinear circuits driven by two-tone signals, use has been made of the describing frequency concept [16], whereby a bilinear transformation is employed to map the two-dimensional frequency grid onto an optimum one-dimensional spectrum. Discrete Fourier transforms can then be employed efficiently once the spectrum gaps typical of modulation problems are removed.

The crucial stage is the definition of the two-dimensional frequency grid, shown in Fig. 4, given by

$$\omega_{m,n} = m\omega_1 + n\omega_2 \tag{6}$$

$$|m| + |n| \leq p \tag{7}$$

with p defined as the order of nonlinearity of the device being analyzed. This means that the device behavior is assumed to be properly assessed when only the Fourier coefficients corresponding to frequencies $\omega_{m,n}$, such that $|m| + |n| \leq p$, are considered in the solution. This assumption is present in any form of the harmonic balance technique and does not limit the validity of the approach.

The original "diamond-shaped" spectrum generated by the commensurable basis frequencies ω_1 and ω_2 (a necessary condition for the method) is then transformed (Fig. 4) to an equivalent one using incommensurable basis frequencies ω_1' and ω_2'. The transformed frequencies are called describing frequencies [16] and, as an important consequence, the corresponding DFT is frequency independent. Furthermore, by choosing

$$\omega_1' = p\omega_0 \tag{8}$$

$$\omega_2' = (p+1)\omega_0 \tag{9}$$

with ω_0 an arbitrary frequency basis, it can be readily seen that the typical spectrum gaps present in modulation problems will not exist. This implies that the two-tone problem is reduced to an equivalent single-tone case and that the total number of frequencies considered is $p(p+1)$. The mapping is relatively simple and its inclusion in a conventional single-tone harmonic balance is straightforward.

The overall harmonic balance procedure has bee implemented and the solution process shows extremely fast convergence properties for a wide range of nonlinear problems. When simulating power amplifiers it requires fewer than 30 iterations when six harmonics are considered for the single-tone excitation and fewer than 40 iterations considering 30 frequencies ($p = 5$) for the two-tone intermodulation distortion analysis for drive levels corresponding to up to 3 dB of gain compression.

V. Results

Load-pull contours for the NE9000 have been simulated over the 6 to 12 GHz range. The agreement with the measured results [11] is excellent, as can be seen in Fig. 5

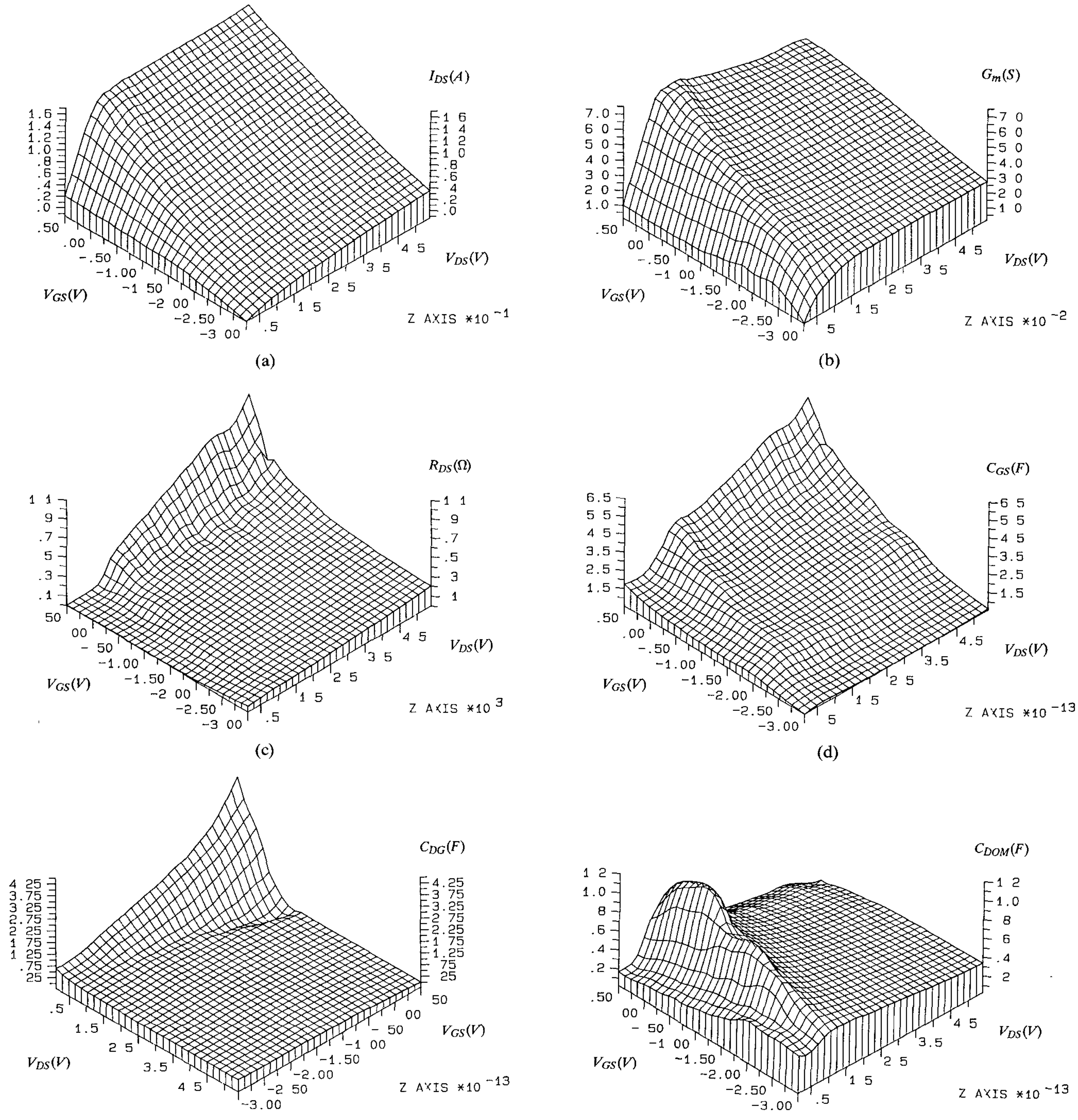


Fig. 3. NE9000 equivalent circuit element values. (a) I_{DS}, (b) G_m, (c) R_{DS}, (d) C_{GS}, (e) C_{DG}, and (f) C_{DOM}. Bias range is $V_{GS} = -3.0$ to $+0.5$ V and $V_{DS} = 0$ to 5.0 V.

where load-pull contours of gain (Fig. 5(a)) and output power (Fig. 5(b)) corresponding to the 1 dB compression point are shown.

Fig. 6 shows the simulated results of the two-tone procedure with signals at 9.99 and 10.00 GHz with equal input powers (again for 1 dB compression). It can be seen that both the gain and output power contours are similar in shape to those in Fig. 5, but an output power compression effect can be clearly seen whereby for the same values of gain at the 1 dB compression point in both the single- and two-tone situations (Figs. 5(a) and 6(a)), the corresponding output powers differ by 5 dB (Figs. 5(b) and 6(b)). Fig. 6(c) and (d) shows intermodulation distortion contours for both a low drive level (10 dB below 1 dB compression) and for the 1 dB compression point. It is evident that there is a tendency for the optimum load termination for minimum IMD to move toward the center of the chart as the power is increased.

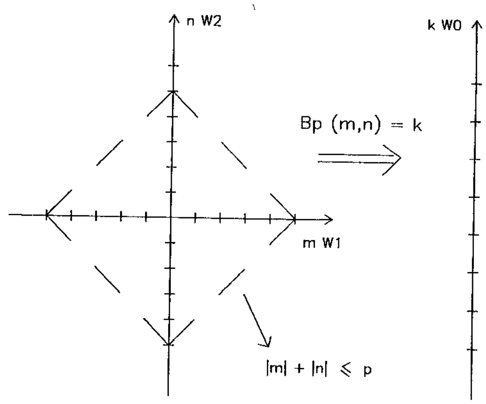
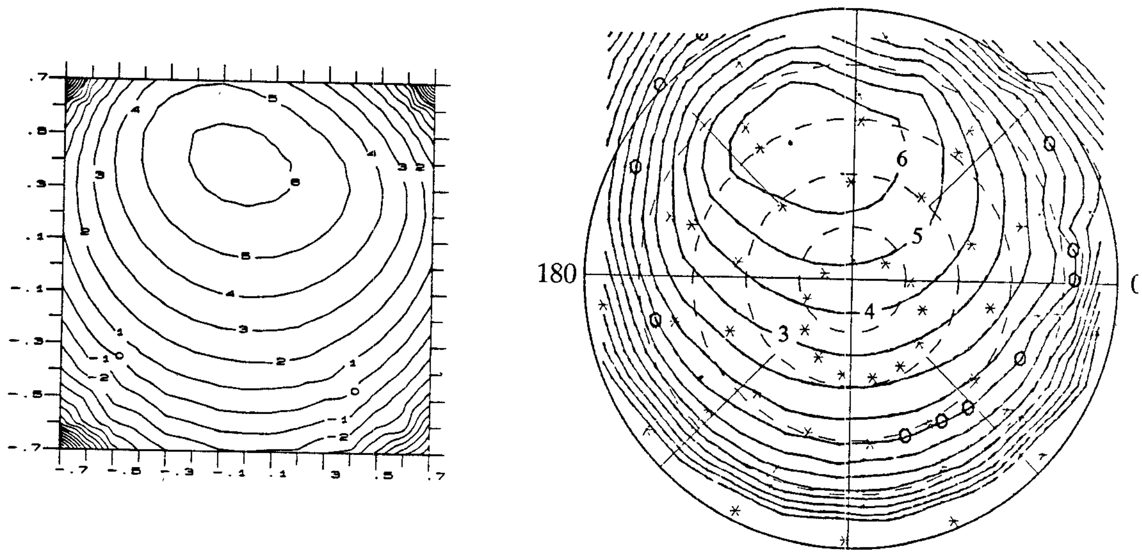
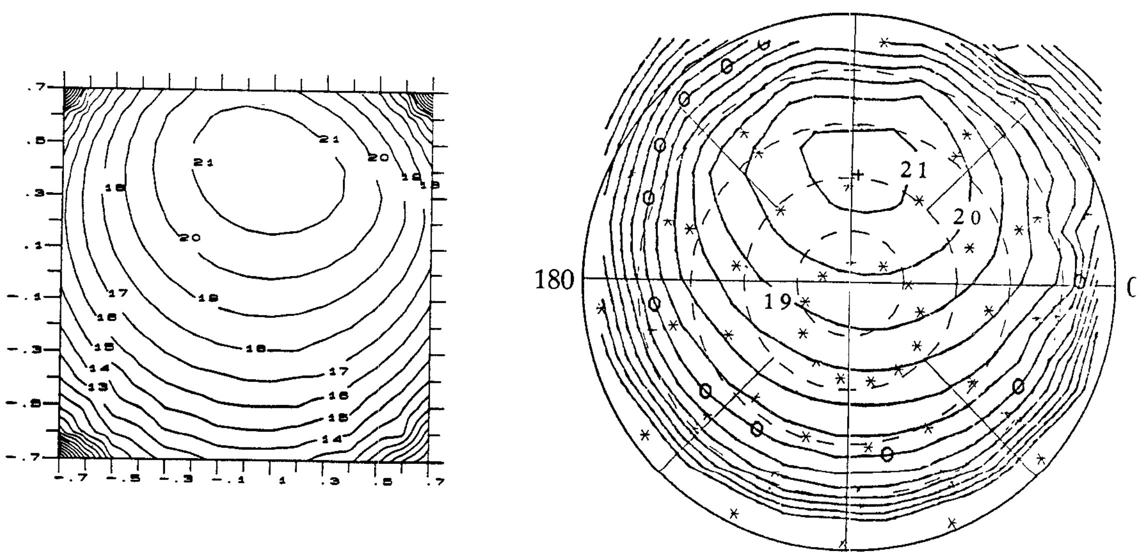


Fig. 4. Bilinear transformation of the two-dimensional frequency grid onto an equivalent one-dimensional spectrum.



(a)



(b)

Fig. 5. Measured and simulated load-pull contours of (a) gain and (b) output power at the 1 dB compression point.

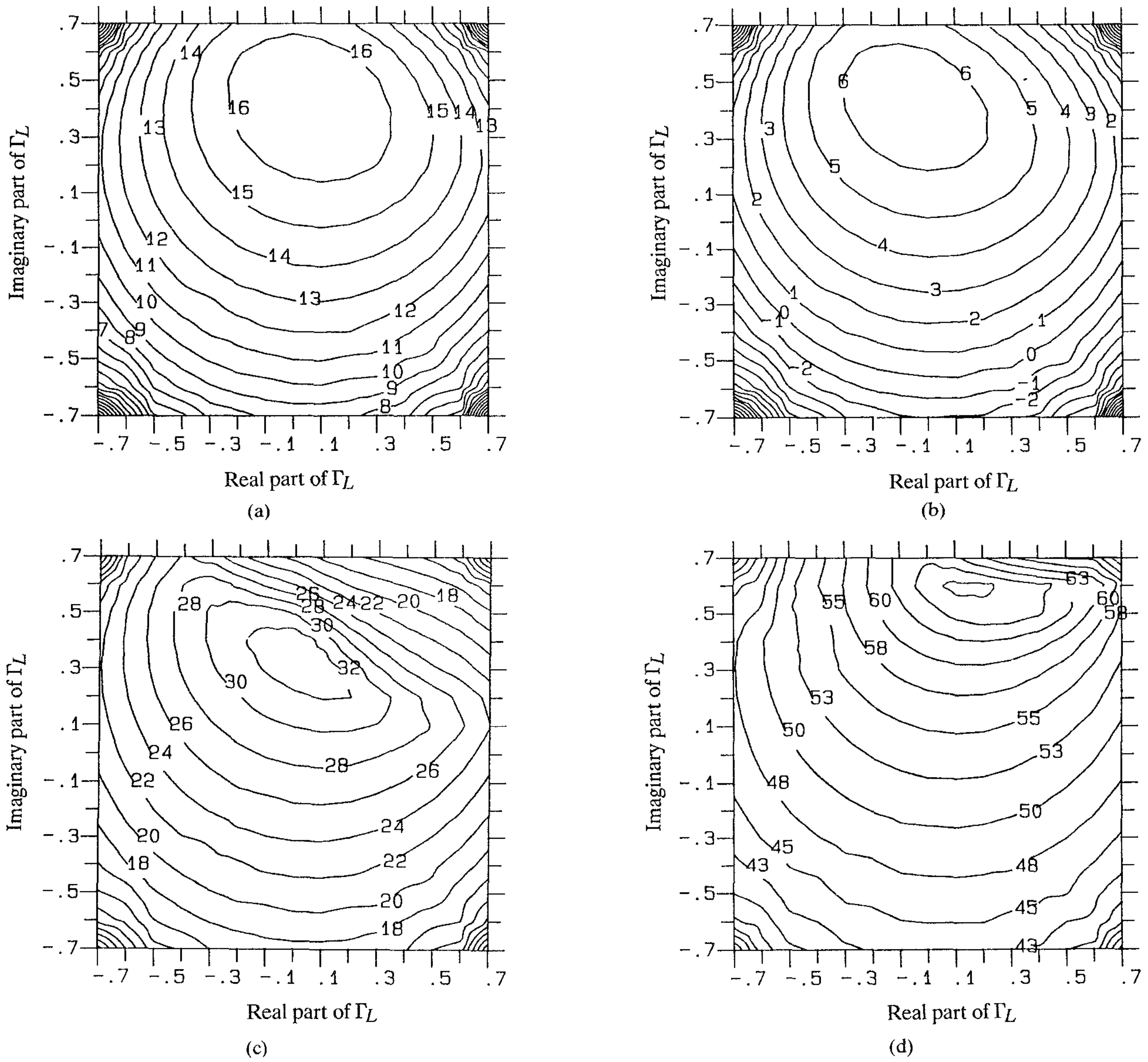


Fig. 6. Simulated two-tone harmonic balance load-pull contours of (a) gain, (b) output power at the 1 dB compression point, (c) IMD at the 1 dB compression point, and (d) IMD contours at 10 dB below the 1 dB compression point.

VI. Conclusions

A quasi-static, large-signal MESFET model based on a quasi-two-dimensional device physical simulation has been developed and combined with a single/two-tone harmonic balance analysis procedure. Application of the describing frequency concept drastically reduced the complexity of the two-tone excitation problem by transforming it to an equivalent single-tone case. Numerical load-pull contours, as well as intermodulation distortion contours, have been simulated and excellent agreement with experimental results has been demonstrated.

References

[1] T. Wada and J. Frey, "Physical basis of short-channel MESFET operation," *IEEE Solid-State Circuits*, vol. SC-14, pp. 398–411, Apr. 1979.

[2] W. R. Curtice and Y. Yun, "A temperature model for the GaAs MESFET," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 954–962, Aug. 1981.

[3] R. K. Cook and J. Frey, "Two-dimensional numerical simulation of energy transport effects in Si and GaAs MESFETs," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 970–977, June 1982.

[4] C. M. Snowden, M. J. Howes, and D. V. Morgan, "Large-signal model of GaAs MESFET operation," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1817–1824, Dec. 1983.

[5] C. M. Snowden and D. Loret, "Two-Dimensional hot-electron models for short-gate-length GaAs MESFETs," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 212–223, Feb. 1987.

[6] K. Blotekjaer, "Transport equations for electrons in two-valley semiconductors," *IEEE Trans. Electron Devices*, vol. ED-17, pp. 38–47, Jan. 1970.

[7] R. R. Pantoja, M. J. Howes, J. R. Richardson, and C. M. Snowden, "The design of microwave subsystems based on a physical device model," in *Proc. IEEE Int. Symp. Circuits Syst.* (Finland), June 1988, pp. 2065–2068.

[8] C. M. Snowden and R. R. Pantoja, "Quasi-two-dimensional simulations for CAD," *IEEE Trans. Electron Devices*, vol. 36, Sept. 1989.

[9] B. Carnez, A. Cappy. A. Kaszynski, E. Constant, and G. Salmer, "Modelling of submicrometer gate field-effect transistor including effects of non-stationary electron dynamics." *J. Appl. Phys.*, vol. 51, pp. 784–790, 1980.

[10] P. A. Sandborn, J. R. East, and G. I. Haddad, "Quasi-two-dimensional modeling of GaAs MESFETs" *IEEE Trans. Electron Devices*, vol. ED-34, pp. 985–991, May 1987.

[11] M. Pierpoint, "Simulation and characterisation of GaAs MESFETs for power amplifier application," Ph.D. dissertation, University of Leeds, Leeds, U. K., 1987.

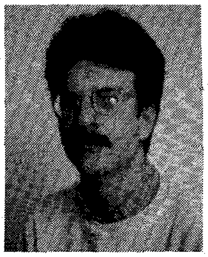
[12] L. Ricco, G. P. Locatelli, and F. Calzavara, "Constant intermodulation loci measure for power devices using HP8510 network analyser," in *1988 IEEE MTT-S Int. Microwave Symp. Dig.* (New York), June 1988, pp. 221–224.

[13] K. Kundert and A. Sangiovanni-Vicentelli, "Simulation of nonlinear circuits in the frequency domain," *IEEE Trans. Computer-Aided Design* vol CAD-5, pp. 521–535, Oct. 1986.

[14] V. Rizzoli and A. Neri, "State of the art and present trends in nonlinear microwave CAD techniques," *IEEE Trans. Microwave Theory Tech.* vol. 36, pp. 343–365, Feb. 1988.

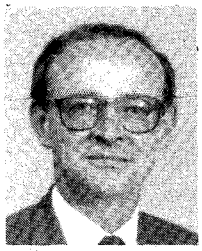
[15] C. Camacho-Penalosa, "Numerical steady-state analysis of nonlinear microwave circuits with periodic excitation," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 724–730, Sept. 1983

[16] D. Hente and R. H. Jansen, "Frequency domain continuation method for the analysis and stability investigation of nonlinear microwave circuits," *Proc. Inst. Elec. Eng.* vol. 133, pt. H, pp. 351–362, Oct. 1986.



Renato R. Pantoja was born in Rio de Janeiro, Brazil, on March 14, 1961. He received the B.Sc. and M.Sc. degrees from the Military Engineering Institute in 1983 and 1986, respectively.

After graduating he worked as a Research Assistant at the Military Engineering Institute on the development of broad-band microwave voltage-controlled oscillators and antennas. He joined the Microwave Solid State Group at Leeds University, Leeds, U.K., in 1986, where he is currently studying for the Ph.D. degree. His main research interests are the nonlinear characterization of MESFET's incorporated into large-signal microwave circuits.



Michael J. Howes (SM'83), who is 47 and married with one child, was born in Lowestoft, Suffolk, England. A student at the University of Leeds, Leeds, U.K., during the 1960's, he gained a first in electronic engineering in 1965 and received the Ph.D degree two years later, having previously worked for the Ministry of Agriculture, Fisheries and Food developing new electronic systems for use in oceanographic studies and fish shoal detection.

In 1967 he was appointed Lecturer in Electronic Engineering at Leeds and promoted to a senior lectureship in 1976. He has had a great deal of industrial experience both in the United States and the U.K., where from 1980 to 1982 he was the Technical Director of MM Microwave, Kirkbymoorside, Yorkshire, England. He became Head of the Department of Electrical and Electronic Engineering at Leeds University in 1984 and Professor of Electronic Engineering in 1988. In 1969 he set up a Microwave Solid-State Research Group anticipating the importance of high-speed and high-frequency integrated circuits in future radar and communication systems. The research group now has 40 active research workers, most of whom are working on collaborative projects with industrial establishments throughout the world. His personal research interests are concerned with the design of microwave devices and subsystems, with a particular interest in the computer-aided design of monolithic integrated circuits. He has also been actively involved in professional further education and is closely involved in the Leeds Microwave Summer School, which attracts 100 industrialists every year for intensive updating in modern electronic system design.

Dr. Howes has published over 100 scientific papers and 16 books, and is currently the European Editor of *Microwave Systems News*. He has lectured widely all over the world and in 1980 was a Visiting Professor at Cornell University, Ithaca, NY. He is a fellow of the IEE and a member of the Institute of Physics.

John R. Richardson (M'58) was born in Durham, England, in 1930 and spent his undergraduate and postgraduate student years at Leeds University from 1949 to 1955, when he emigrated to Canada.

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Christopher M. Snowden (S'82–M'82) was born in Hull, England, on March 5, 1956. He received the B.Sc., M.Sc., and Ph.D. degrees from the University of Leeds, Leeds, England. His Ph.D. studies were conducted in association with Racal-MESL and were concerned with the large-signal characterization of MESFET oscillators.

After graduating he worked as an Applications Engineer for Mullard, Mitcham. In 1982, he was appointed Lecturer in the Department of Electronics at the University of York. He joined the Microwave Solid State Group in the Department of Electrical and Electronic Engineering at the University of Leeds in July 1983, where he is currently a Senior Lecturer. During 1987 he was a Visiting Research Associate at the California Institute of Technology. His main research interests include semiconductor device modeling, nonlinear subsystem design and characterization, and advanced semiconductor devices.

Dr. Snowden is a founding member of the International GaAs Simulation Group.